**WHAT IS CLAIMED IS:**

1. A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor; and

a first interconnection layer formed on the interlevel dielectric film,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode.

2. The device of Claim 1, wherein the first interconnection layer includes:

a storage line connected to the top electrode of the ferroelectric capacitor and to the first doped layer of the memory cell transistor, the storage line having a linear pla-

nar pattern; and

a bit line connected to the second doped layer of the memory cell transistor, and

wherein the storage line intersects only one side of the top electrode in the planar layout.

3. The device of Claim 2, wherein the storage line includes:

a first region connected to the top electrode of the ferroelectric capacitor;

a second region connected to the first doped layer of the memory cell transistor; and

a third region being interposed between the first and second regions and intersecting the side of the top electrode in the planar layout, and

wherein the line width of the third region is smaller than that of the first and second regions.

4. The device of Claim 2, wherein the bit line does not overlap with the top electrode in the planar layout.

5. The device of Claim 4, wherein the storage line includes:

a first region connected to the top electrode of the ferroelectric capacitor;

a second region connected to the first doped layer of the memory cell transistor; and

a third region being interposed between the first and second regions and intersecting the side of the top electrode in the planar layout, and

wherein the line width of the third region is smaller than that of the first and second regions.

6. The device of Claim 1, wherein the first interconnection layer includes:

a storage line connected to the top electrode of the ferroelectric capacitor and to the first doped layer of the memory cell transistor, the storage line having a linear planar pattern; and

a bit line connected to the second doped layer of the memory cell transistor, and

wherein the bit line does not overlap with the top electrode in the planar layout.

7. The device of Claim 1, wherein the first interconnection layer is made of a material containing at least one of aluminum and copper.

8. The device of Claim 1, further comprising:

an upper interlevel dielectric film formed to cover the

first interconnection layer; and

a second interconnection layer formed on the upper interlevel dielectric film,

wherein the second interconnection layer totally covers the top electrode of the ferroelectric capacitor in the planar layout.

9. The device of Claim 1, further comprising:

an upper interlevel dielectric film formed to cover the first interconnection layer; and

a second interconnection layer formed on the upper interlevel dielectric film,

wherein the second interconnection layer totally covers the bottom electrode of the ferroelectric capacitor in the planar layout.

10. The device of Claim 9, wherein the second interconnection layer is made of a material containing at least one of aluminum and copper.

add C3)